EE 505 Experiment 4 Spring 2025

Dynamic Comparators

Comparators are a critical component in the design of any ADC. Though operational amplifiers can be used for comparators, they are often not fast enough and near the transition point of the comparator, the gain is not high enough to force a valid Boolean signal at the output of the amplifier. Many ADC architectures will also be clocked with an expectation that the comparators make a decision when the clock signal transitions from either high to low or low to high. Some form of regenerative feedback is usually used for building comparators used in ADCs to help ensure a transition near the trip point and to ideally speed up the response of the comparator.

One of the most simple dynamic comparators is shown in Figure 1.

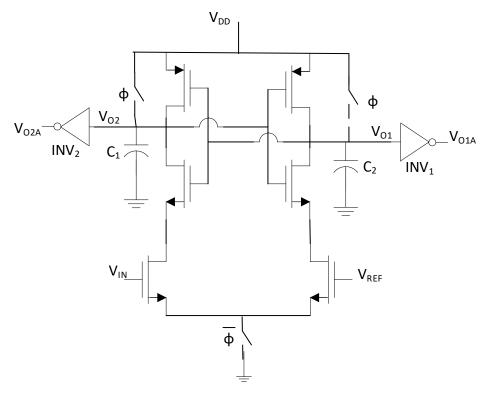


Figure 1: Simple dynamic comparator schematic

- 1. Design this amplifier with minimum-sized devices and determine the off voltage. Initially neglect the load capacitors C1 and C2 and the Inverters.
- 2. How does the offset voltage change if C2 and C1 are 500fF capacitors? What effect does changing C1 to 510fF have on the offset voltage.
- 3. What happens to the offset voltage if one inverter, the one on the right, is added to post-process the Boolean output?